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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,894	SHIMAMURA, AKIMITSU	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☒ Claim(s) *1-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been considered. Claims 1 and 14 have been amended as per Applicant's request.

Claim Objections

2. Claims 1-24 are objected to because of the following informalities: There are several grammatical and language clarification informalities. Please see the suggested corrections below which highlight the informalities and suggest an appropriate change to correct the informality. Appropriate correction is required.

1. A computer system employing a pipeline operation wherein the pipeline is driven by a high clock frequency higher than a low clock frequency by which a critical path instruction in processing data can be executed correctly, comprising:
   a. A high frequency ALU driven by high clock frequency, a low frequency ALU driven by the low clock frequency by which, during the low clock frequency, the critical path instruction can be executed correctly, wherein
   b. If the high frequency ALU can execute an execution stage instruction correctly, ~~the~~ an execution result of the high frequency ALU is output as an execution result of a pipeline execution stage,
   c. If the high frequency ALU can not execute the execution stage instruction correctly, ~~the~~ an execution result of the low frequency ALU is output as ~~an~~ the execution result of the pipeline execution stage instead of the execution result of the high frequency ALU.
2. The computer system according to claim 1,
   a. Wherein the low frequency ALU is composed of ~~plural~~ a plurality of low frequency ALUs;
   b. ~~The~~ A low frequency ALU in the plurality of low frequency ALUs in charge of each execution stage is switched in turn, and each of

the plurality of low frequency ALUs in charge executes ~~an~~ the execution stage instruction ~~in charge~~ correctly by the low clock frequency which is equal to or lower than ~~the~~ a clock frequency for operating ~~a~~ the critical path instruction correctly.

3. The computer system according to claim 2,

   a. Wherein ~~the number of~~ the plurality of low frequency ALUs is equal to "n" low frequency ALUs when the ~~pipeline~~ high clock frequency is "n" times of the low clock frequency by which the critical path instruction can be executed correctly,

   b. Each of the ~~"n" pieces of the~~ plurality of low frequency ALUs is in charge of "n" pieces of the pipeline execution stage ~~execution stages of pipeline~~ in order respectively.

4. The computer system according to claim 3, further comprising

   a. A comparator comparing the ~~output~~ result of the high frequency ALU and the ~~output~~ result of the low frequency ALU in charge of ~~the~~ a same execution stage for ~~the~~ a same instruction,

   b. Wherein, the ~~output~~ result of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when ~~the compared~~ a comparison result of the comparator indicates matching, the ~~output~~ result of the high frequency ALU is determined as the execution result of the execution stage and ~~the~~ pipeline operation is continued, and when the ~~compared~~ comparison result of the comparator indicates mismatching, the ~~output~~ result of the high frequency ALU is replaced with the ~~output~~ result of the low frequency ALU as the execution result of the pipeline execution stage.

5. The computer system according to claim 4, wherein when the ~~compared~~ comparison result of the comparator indicates mismatching, all stages of the pipeline are stopped until finishing ~~the~~ a replacement process in which the ~~output~~ result of the low frequency ALU is selected as the execution result of the pipeline

execution stage.

6. The computer system according to claim 2, further comprising

a. A comparator comparing the ~~output~~ result of the high frequency ALU and the ~~output~~ result of the low frequency ALU in charge of ~~the~~ a same execution stage for ~~the~~ a same instruction,

~~a)~~b. Wherein, the ~~output~~ result of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when ~~the compared~~ a comparison result of the comparator indicates matching, the ~~output~~ result of the high frequency ALU is determined as the execution result of the execution stage and ~~the~~ pipeline operation is continued, and when the ~~compared~~ comparison result of the comparator indicates mismatching, the ~~output~~ result of the high frequency ALU is replaced with the ~~output~~ result of the low frequency ALU as the execution result of the pipeline execution stage.

7. The computer system according to claim 6, wherein when the ~~compared~~ comparison result of the comparator indicates mismatching, all stages of the pipeline are stopped until finishing ~~the~~ a replacement process in which the ~~output~~ result of the low frequency ALU is selected as the execution result of the pipeline execution stage.

8. The computer system according to claim 1 further comprising

a. A comparator comparing the ~~output~~ result of the high frequency ALU and the ~~output~~ result of the low frequency ALU in charge of ~~the~~ a same execution stage for ~~the~~ a same instruction,

~~a)~~b. Wherein, the ~~output~~ result of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when ~~the compared~~ a comparison result of the comparator indicates matching, the ~~output~~ result of the high frequency ALU is determined as the execution result of the execution stage and ~~the~~ pipeline operation is continued, and when the ~~compared~~ comparison

result of the comparator indicates mismatching, the ~~output~~ result of the high frequency ALU is replaced with the ~~output~~ result of the low frequency ALU as the execution result of the pipeline execution stage.

9. The computer system according to claim 8, wherein when the ~~compared~~ comparison result of the comparator indicates mismatching, all stages of the pipeline are stopped until finishing ~~the~~ a replacement process in which the ~~output~~ result of the low frequency ALU is selected as the execution result of the pipeline execution stage.

10. The computer system according to claim 1, further comprising a counter counting ~~the~~ a number of occurrences of ~~the~~ a mismatching detection signal in a predetermined period, and a circuit varying ~~the~~ a pipeline clock frequency according to the ~~counted~~ number of occurrences.

11. The computer system according to claim 1,

a. Wherein ~~the following~~ amounts of two processes are compared when ~~the~~ a pipeline clock frequency is increased and ~~the~~ a number of the critical path instructions is increased, ~~the one~~ a first amount being an improved process amount of the high frequency ALU and ~~the other~~ a second amount being a deteriorated process amount ~~by increasing of the~~ that increases if a replacement process ~~of~~ uses the ~~output~~ result of the low frequency ALU as the execution result of the pipeline execution stage when the high frequency ALU cannot execute the execution stage instruction correctly,

~~a)~~b. Wherein, when the ~~former~~ first amount is larger than the ~~latter~~ second amount by ~~the~~ a predetermined amount, the pipeline clock frequency is increased.

12. The computer system according to claim 1,

a. Wherein~~, the following~~ amounts of two processes are compared when ~~the~~ a pipeline clock frequency is decreased and ~~the~~ a number of the critical path instructions is decreased, ~~the one~~ a first amount

being a deteriorated process amount of the high frequency ALU if ~~the~~ a pipeline clock frequency is lowered, and ~~the other~~ a second amount being an improved process amount ~~by decreasing of the~~ that decreases if a replacement process ~~of~~ uses the ~~output~~ result of the low frequency ALU as the execution result of the pipeline execution stage when the high frequency ALU cannot execute the instruction correctly,

~~a)~~b. Wherein, when the ~~latter~~ first amount is larger than the ~~former~~ second amount by a predetermined amount, the pipeline clock frequency is decreased.

13. The computer system according to claim 1 further comprising plural ALUs, a data generation circuit generating test data as a critical path data, an execution time measurement circuit measuring the critical path instruction in each ALU, and a detector detecting ~~the fastest~~ which ALU ~~that can execute~~ executes the critical path instruction in a shortest time,

a. Wherein, ~~the~~ a faster ALU detected by the detector is selected as the high frequency ALU, and ~~the other one~~ a slower ALU or ~~plural~~plurality of slower ALUs is/are selected as the low frequency ALU/ALUs.

14. A method for controlling a pipeline operation in a computer system

a. Wherein ~~the~~ a pipeline is driven by a high clock frequency higher than a low clock frequency by which a critical path instruction ~~in processing data~~ can be executed correctly, comprising:

i. Using a high frequency ALU driven by ~~the~~ a high clock frequency, a low frequency ALU driven by ~~the~~ a low clock frequency by which the low clock frequency executes the critical path instruction ~~can be executed~~ correctly, wherein

ii. If the high frequency ALU can execute an execution stage instruction correctly outputting ~~the~~ an execution result of the high frequency ALU as an execution result of a pipeline

execution stage,

iii. If the high frequency ALU can not execute the execution stage instruction correctly, outputting the execution result of the low frequency ALU as ~~an~~ the execution result of the pipeline execution stage instead of the execution result of the high frequency ALU.

15. The method for controlling a pipeline operation in a computer system according to claim 14,

a. Wherein the low frequency ALU is composed of ~~plural~~ a plurality of low frequency ALUs;

b. Switching ~~the~~ one of the plurality of low frequency ~~ALU~~ ALUs in charge of each execution stage in turn, and assigning each of the plurality of low frequency ~~ALU~~ ALUs in charge for an execution stage instruction ~~in charge~~ to execute ~~it~~ the execution stage instruction correctly ~~by~~ during the low clock frequency which is equal to or lower than ~~the~~ a clock frequency for operating ~~a~~ the critical path instruction correctly.

16. The method for controlling a pipeline operation in a computer system according to claim 15,

a. Wherein ~~the number of~~ the ~~plural~~ plurality of low frequency ALUs is equal to "n" low frequency ALUs when the ~~pipeline~~ high clock frequency is "n" times of the low clock frequency by which the critical path instruction can be executed correctly,

b. Each of ~~the "n" pieces of~~ the plurality of low frequency ALUs is in charge of "n" pieces of ~~execution stages of pipeline~~ the pipeline execution stage in order respectively.

17. The method for controlling a pipeline operation in a computer system according to claim 16, further comprising ~~comparing method for~~ comparing the ~~output~~ result of the high frequency ALU and the ~~output~~ result of the low frequency ALU in charge of ~~the~~ a same execution stage for ~~the~~ a same instruction,

a. Wherein, the ~~output~~ result of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when ~~the compared~~ a comparison result indicates matching, the ~~output~~ result of the high frequency ALU is determined as the execution result of the execution stage and ~~the~~ pipeline operation is continued, and when the ~~compared~~ comparison result indicates mismatching, the ~~output~~ result of the high frequency ALU is replaced with the ~~output~~ result of the low frequency ALU as the execution result of the pipeline execution stage.

18. The method for controlling a pipeline operation in a computer system according to claim 17, wherein when the ~~compared~~ comparison result indicates mismatching, all stages of the pipeline are stopped until finishing ~~the~~ a replacement process in which the ~~output~~ result of the low frequency ALU is selected as the execution result of the pipeline execution stage.

19. The method for controlling a pipeline operation in a computer system according to claim 15, further comprising ~~a comparing method for~~ comparing the ~~output~~ result of the high frequency ALU and the ~~output~~ result of the low frequency ALU in charge of ~~the~~ a same execution stage for ~~the~~ a same instruction,

a. Wherein, the ~~output~~ result of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when ~~the compared~~ a comparison result indicates matching, the ~~output~~ result of the high frequency ALU is determined as the execution result of the execution stage and ~~the~~ pipeline operation is continued, and when the ~~compared~~ comparison result indicates mismatching, the ~~output~~ result of the high frequency ALU is replaced with the ~~output~~ result of the low frequency ALU as the execution result of the pipeline execution stage.

20. The method for controlling a pipeline operation in a computer system according to claim 19, wherein when the ~~compared~~ comparison result indicates mismatching, all stages of the pipeline are stopped until finishing ~~the~~ a

replacement process in which the ~~output~~ result of the low frequency ALU is selected as the execution result of the pipeline execution stage.

21. The method for controlling a pipeline operation in a computer system according to claim 14 further comprising ~~a comparing method for~~ comparing the ~~output~~ result of the high frequency ALU and the ~~output~~ result of the low frequency ALU in charge of ~~the~~ a same execution stage for ~~the~~ a same instruction,

a. Wherein, the ~~output~~ result of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when ~~the~~ ~~compared~~ a comparison result indicates matching, the ~~output~~ result of the high frequency ALU is determined as the execution result of the execution stage and ~~the~~ pipeline operation is continued, and when the ~~compared~~ comparison result indicates mismatching, the ~~output~~ result of the high frequency ALU is replaced with the ~~output~~ result of the low frequency ALU as the execution result of the pipeline execution stage.

22. The method for controlling a pipeline operation in a computer system according to claim 21, wherein when the ~~compared~~ comparison result indicates mismatching, all stages of the pipeline are stopped until finishing ~~the~~ a replacement process in which the ~~output~~ result of the low frequency ALU is selected as the execution result of the pipeline execution stage.

23. The method for controlling a pipeline operation in a computer system according to claim 14, further comprising ~~a counting method for~~ counting ~~the~~ a number of occurrences of ~~the~~ a mismatching detection signal in a predetermined period, and ~~a method for~~ varying ~~the~~ a pipeline clock frequency according to the ~~counted~~ number of occurrences.

24. The method for controlling a pipeline operation in a computer system according to claim 14,

a. Wherein ~~the following~~ amounts of two processes are compared when ~~the~~ a pipeline clock frequency is increased and ~~the~~ a number of the critical path instructions is increased, ~~the one~~ a first amount

being an improved process amount of the high frequency ALU and ~~the other~~ a second amount being a deteriorated process amount ~~by increasing of the~~ that increases if a replacement process ~~of~~ uses the ~~output~~ result of the low frequency ALU as the execution result of the pipeline execution stage when the high frequency ALU cannot execute the instruction correctly,

~~a)~~b. Wherein, when the ~~latter~~ first amount is larger than the ~~latter~~ second amount by ~~the~~ a predetermined amount, the pipeline clock frequency is increased.

25. The method for controlling a pipeline operation in a computer system according to claim 14,

a. Wherein~~, the following~~ amounts of two processes are compared when ~~the~~ a pipeline clock frequency is decreased and ~~the~~ a number of the critical path instructions is decreased, ~~the one~~ a first amount being a deteriorated process amount of the high frequency ALU if the pipeline clock frequency is lowered, and ~~the other~~ a second amount being an improved process amount ~~by decreasing of the~~ that decreases if a replacement process ~~of~~ uses the ~~output~~ result of the low frequency ALU as the execution result of the pipeline execution stage when the high frequency ALU cannot execute the instruction correctly,

~~a)~~b. Wherein, when the ~~latter~~ first amount is larger than the ~~former~~ second amount by a predetermined amount, the pipeline clock frequency is decreased.

26. The method for controlling a pipeline operation in a computer system according to claim 14, using plural ALUs, further comprising ~~a method for~~ generating test data as a critical path data, ~~a method for~~ measuring the critical path instruction in each ALU, and ~~a method for~~ detecting ~~the fastest~~ which ALU that ~~can execute~~ executes the critical path instruction in a shortest time,

a. Wherein, ~~the~~ a faster detected ALU is selected as the high

frequency ALU, and ~~the other one~~ a slower ALU or ~~plural~~ plurality of slower ALUs is/are selected as the low frequency ALU/ALUs.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. There are numerous 35 USC §112, second paragraph insufficient antecedent basis for limitations in the claims throughout all the claims. Below are a few examples of the insufficient antecedent basis for the limitations in the claims problems. The proposed claim amendments above fix most of these problems. However, the Applicant and/or Applicant's representative is encouraged to review the claims and correct the 35 USC §112 problems.

5. Claim 1 recites the limitations "the execution result of the high frequency ALU" in lines 7-8 and "the instruction" in line 9. There is insufficient antecedent basis for this limitation in the claim. There is no previous "execution result of the high frequency ALU" in the claim and it is unclear which instruction, the critical path instruction or instruction being executed, is being referred to.

6. Claim 2 recites the limitation "The low frequency ALU" in line 3. There is insufficient antecedent basis for this limitation in the claim. It is unclear whether the entire plurality of low frequency ALUs or a single low frequency ALU in the plurality of low frequency ALUs is being referred to.

7. Claim 3 recites the limitation "the pipeline clock frequency" in lines 2-3 and "the clock frequency" on lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

There is no previous "pipeline clock frequency" or "clock frequency" in the claim nor is it clear whether they are referring to the high clock frequency of the low clock frequency.

8. Claim 4 recites the limitations "the output of the high frequency ALU" and "the output of the low frequency ALU" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. There are no previous outputs of the high and low frequency ALUs.

9. Claim 5 recites the limitation "the replacement process" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. There is no previous replacement process established in the claim.

10. Claim 10 recites the limitations "the number of occurrences" in line 2 and "the mismatching detection signal" in line 2. There is insufficient antecedent basis for this limitation in the claim. There are no previous "number of occurrences" or "mismatching detecting signal" established in the claim.

11. Claim 11 recites the limitations "the follow amounts of two processes" in lines 1-2, "the number of the critical path instructions" in lines 2-3, "the one" in line 3, "the other" in line 4, "the replacement process" in lines 4-5, "the former" in line 7, "the latter" in line 7, and "the predetermined amount" in line 7. There is insufficient antecedent basis for this limitation in the claim. None of these limitations have been established previously in the claim.

12. Claim 13 recites the limitation "the ALU detected by the detector" in line 3. There is insufficient antecedent basis for this limitation in the claim. It is unclear which ALU, the slower or the faster ALU, is being referred to by this limitation.

13. Claims 6-9, 12, and 14-26 are duplicates of the ones above, list the same limitations, and/or are merely the method version of the apparatus claims above. The same 35 USC §112,

second paragraphs that applied to the claims and limitations above apply to the similar claims and limitations in the duplicate/similar claims/limitations.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1 and 14 are rejected under 35 U.S.C. 102(b) as being taught by Carnevale et al., U.S. Patent Number 3,656,123 (herein referred to as Carnevale).

16. Referring to claim 1, Carnevale has taught a computer system employing a pipeline operation wherein the pipeline is driven by a high clock frequency higher than a low clock frequency by which a critical path instruction in processing data can be executed correctly (Carnevale column 2, line 68 to column 3, line 6; column 3, lines 16-24 and 31-52; column 3, line 70 to column 4, line 14), comprising:

a. A high frequency ALU driven by high clock frequency, a low frequency ALU driven by the low clock frequency by which low clock frequency the critical path instruction can be executed correctly (Carnevale column 2, line 68 to column 3, line 6; column 3, lines 16-24 and 31-52; column 3, line 70 to column 4, line 14; column 8, lines 21-35; column 24, lines 12-16, 34-58, and 65-69; column 24, lines 1-39; Figure 1; Figure 3; and Figure 5), wherein

b. If the high frequency ALU can execute an instruction correctly, the execution result of the high frequency ALU is output as an execution result of a pipeline

execution stage (Carnevale column 2, line 68 to column 3, line 6; column 3, lines 16-24 and 31-52; column 3, line 70 to column 4, line 14; column 8, lines 21-35; column 24, lines 12-16, 34-58, and 65-69; column 24, lines 1-39; Figure 1; Figure 3; and Figure 5),

c. If the high frequency ALU can not execute the instruction correctly, the execution result of the low frequency ALU is output as an execution result of the pipeline execution stage instead of the execution result of the high frequency ALU (Carnevale column 2, line 68 to column 3, line 6; column 3, lines 16-24 and 31-52; column 3, line 70 to column 4, line 14; column 8, lines 21-35; column 24, lines 12-16, 34-58, and 65-69; column 24, lines 1-39; Figure 1; Figure 3; and Figure 5).

17. In regards to Carnevale, by changing the clock frequency of the system depending on the amount of time an instruction needs makes it necessary for the result of the current time period, which is either at a higher or lower clock frequency, the result used. So, if a lower clock speed is used, like that for move/store instructions, than the lower clock speed results from the ALU must be used instead of the higher clock speed results, since those are the only results.

18. Claim 14 has substantially the same limitations except worded for a method claim instead of the apparatus of claim 1. Therefore, claim 14's matching limitations to claim 1 are rejected under the same art.

Conclusion

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
18 April 2005

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